At the same time, the HL Comp signal out of G10 turns on gate G11. Signals from a 1 MHz oscillator then pass through gate G11 to the first stage of a decade counter system. Four decade counters, each connected to a binary-coded-decimal thumbwheel switch, make up a digital time delay circuit. Range of the circuit is 0 to 9999 μs with 1 μs resolution. Stability, accuracy, and resolution of the time delay system are dependent on the clock oscillator characteristics.

When the desired time delay is reached by counting pulses from the oscillator, each thumbwheel switch provides a positive-going level transition to the inputs of the 832 NAND gate G13. When all inputs go HIGH, gate G13 changes logic state causing gate G14 to produce a positive going pulse to serve as the trigger signal to the flashlamp high voltage firing circuit as shown in Figures 4 and 5.

The mechanical switches tied to gates G12 and G14 are for manually firing the spectrograph shutter and flashlamp circuits. The switch labeled S will fire only the shutter circuit while the one labeled S/FL will fire both circuits together.

When the piston is reseated at the reservoir end after a compressor shot, the PISTON SEATED switch is closed and gate G2 goes from HIGH to LOW. Then the PTB is reset, the gated oscillator is disabled via its pin 2, gate G10 is disabled via its pin 10, and the decade counters are disabled and reset to a count of zero. One cycle of the pressure transducer control circuits is then complete and the system will be in a standby condition.

Magnetic Pickup

Analog signals from the magnetic pickup are connected to the circuit shown in Figure 7 where they are converted into a digital level pulse train by a LM211D voltage comparator. Connected as shown, the comparator operates on the positive portion of the MPU signal with the reference voltage being ground potential as applied to pin 4. A 1N5223 zener diode on the input pin 3 limits the MPU signal applied to the comparator to a value less than the supply voltage. The output of this comparator is also operated at a level to make it compatible with the logic circuits used. Signals from the comparator are sent to an oscilloscope for recording and to the 844 NAND gate G3.

The first output pulse from the comparator passes through gate G3 and triggers an 850 PTB and an 8601 multivibrator. Triggering the 850 PTB causes its outputs to change logic states. When pin 3 goes from HIGH to LOW, gate G3 is disabled and no more signals from the comparator are allowed to pass.

When the 8601 MV is triggered, its output changes logic states for the duration of the time constant determined by the network tied to pins 11 and 13. The timing is variable by using the 50 kΩ

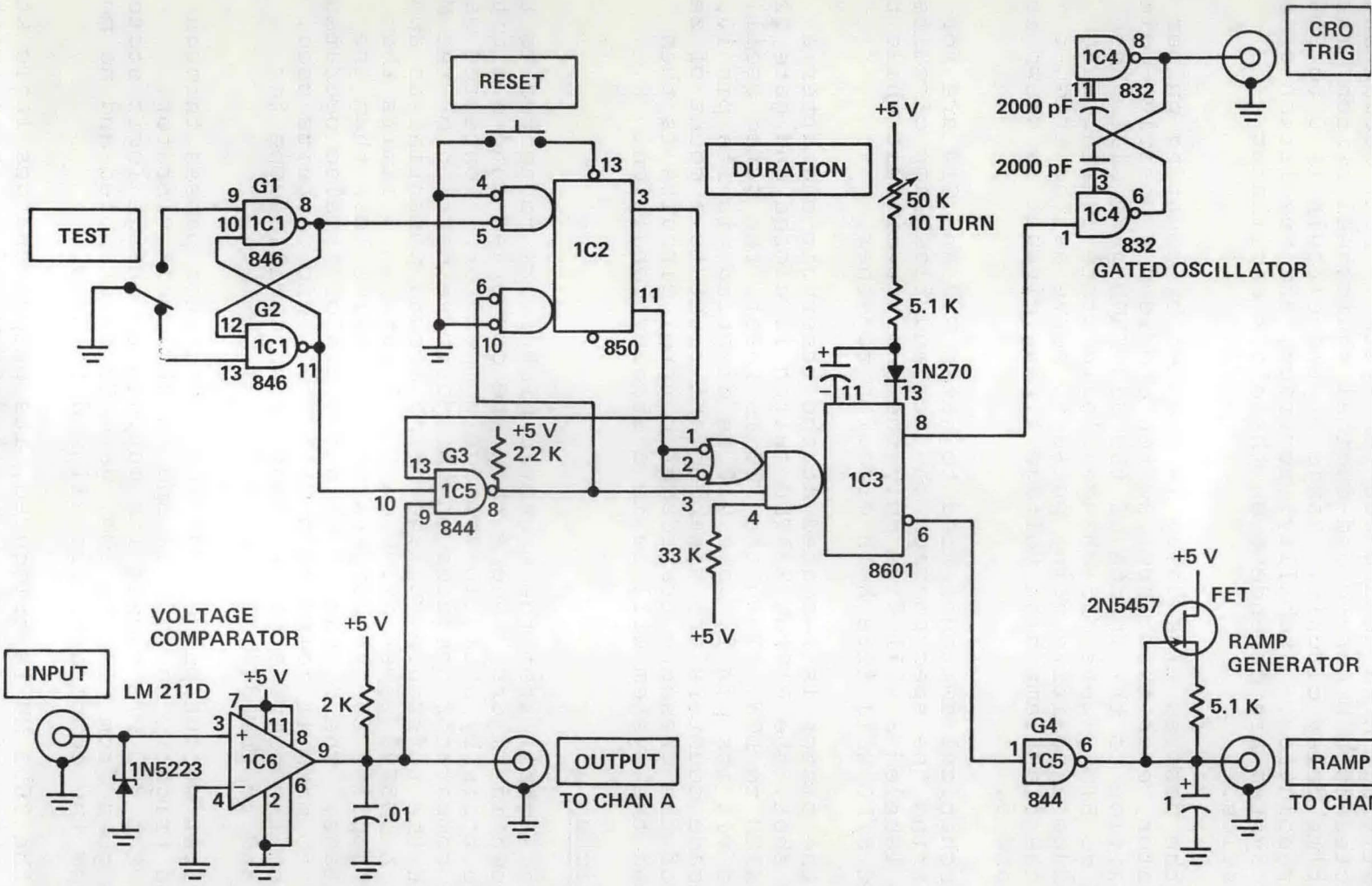

FIG. 7 MAGNETIC PICKUP SIGNAL DISPLAY CIRCUIT